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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/424,966	03/06/2000	AKIHIDE SHIBATA	247322001700	8894

25226 7590 10/08/2002

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EXAMINER
LOKE, STEVEN HO YIN

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 10/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/424,966	SHIBATA ET AL.	
	Examiner	Art Unit	
	Steven Loke	2811	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36* is/are pending in the application.

4a) Of the above claim(s) *4,5,7,9,11,13,15,17,19,21,23,25,27 and 29-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,6,8,10,12,14,16,18,20,22,24,26 and 28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *11 July 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

1. Claims 1-3, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, and 28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, lines 3-5, "a gate terminal fabricated on a channel region, formed between said source region and drain region, which receives a first input signal through a gate insulating film" is unclear whether a gate terminal receives a first input signal and fabricated on a channel region, formed between said source region and drain region, through a gate insulating film.

In claim 1, line 7, the phrase "said well in each of the semiconductor elements is provided with a substrate which receives a second input signal" is unclear whether "said well in each of the semiconductor elements is provided with a substrate terminal which receives a second input signal".

Claim 1 discloses each semiconductor element being provided with a source region having a source terminal and a drain region having a drain terminal. In addition, each of said semiconductor elements is electrically separated from the others. Then it is unclear how a pair of a P-type semiconductor element and an N-type semiconductor element, which make up one of said plurality of semiconductor elements, provided with one source region having one source terminal and one drain region having one drain terminal in claims 6, 10, 18 and 22. There must be two source regions with two source terminals and two drain regions with two drain terminals in a semiconductor element, which composed of a pair of a P-type semiconductor element and an N-type semiconductor element, in claims 6, 10, 18 and 22. It is also unclear whether the P-

type semiconductor element is electrically separated from the N-type semiconductor element in claims 6, 10, 18 and 22.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Okumura et al. (Japanese patent application no. 08-204140).

In regards to claim 1, Okumura et al. shows all the elements of the claimed invention in figs. 1-6. It comprises: a semiconductor device comprising a plurality of semiconductor elements (NMOS and PMOS of fig. 1), each being provided with a source region [105, 107] having a source terminal and a drain region [105, 107] having a drain terminal in a well [104, 106] formed in a semiconductor layer [104, 106], and a gate terminal [109] fabricated on a channel region, formed between the source region and drain region, which receives a first input signal through a gate insulating film [108], wherein: each of the semiconductor elements is electrically separated from the others; and the well in each of the semiconductor elements is provided with a substrate terminal which receives a second input signal from bias generator [207, 208] through a contact hole (see figs. 3 and 6) formed therein at a region [304] other than the source region and drain region [105, 107].

In regards to claim 2, it is inherent that the operating characteristics are changed by adjusting impurity concentration in the channel region and levels of a high voltage and a low voltage applied to the gate terminal and substrate terminal.

In regards to claim 3, the semiconductor layer in each of the semiconductor elements is electrically separated from each other by means of an oxide film [102, 103].

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, 6, 8 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al. in view of Iwamatsu

In regards to claim 1, Chang et al. discloses a CMOS in fig. 1l. It comprises: a semiconductor device comprising a plurality of semiconductor elements, each being provided with a source region [26, 34] and a drain region [23, 32] in a well [8, 12] formed in a semiconductor layer, and a gate terminal [20', 20"] fabricated on a channel region, formed between the source region and drain region, through a gate insulating film [16, 18], wherein: each of the semiconductor elements is electrically separated from the others; and the well in each of the semiconductor elements is provided with a substrate terminal contact hole formed therein at a region [28, 30] other than the source region and drain region.

Chang et al. differs from the claimed invention by not showing a source terminal, a drain terminal and a substrate terminal in each of the semiconductor elements.

It would have been obvious to have a source terminal, a drain terminal and a substrate terminal in each of the semiconductor elements because they provide electrical connection between the semiconductor elements and the external circuit.

Chang et al. further differs from the claimed invention by not showing each gate terminal receives a first input signal and each well receives a second input signal.

Iwamatsu shows each gate terminal [5] receives a first input signal and each well [2, 3] receives a second input signal [V_{BG2}, V_{BG1}] in figs. 1-4.

Since both Chang et al. and Iwamatsu teach a CMOS structure with well contact regions for well voltages, it would have been obvious to have the electrical connections of Iwamatsu in Chang et al. because the well contacts of Chang et al. reduce the electrical resistance between the well terminals and the wells. In addition, the electrical insulation layer [14] of Chang et al. insulates all the terminals of the PMOS, NMOS and the wells.

In regards to claim 2, it is inherent that the operating characteristics are changed by adjusting impurity concentration in the channel region and levels of a high voltage and a low voltage applied to the gate terminal and substrate terminal.

In regards to claim 3, the combined device of Chang et al. and Iwamatsu shows the semiconductor layer in each of the semiconductor elements is electrically separated from each other by means of an oxide film [14].

In regards to claim 6, Chang et al. differs from the claimed invention by not showing a high potential is supplied to a source terminal of the PMOS and a low potential is supplied to a source terminal of the NMOS, the gate terminals of the PMOS and NMOS are connected to each other to form a first input terminal, the substrate terminals of the PMOS and NMOS are connected to each other to form a second input terminal, and the drain terminals of the PMOS and NMOS are connected to each other to form an output terminal.

Iwamatsu shows showing a high potential V_{DD} is supplied to a source terminal of the PMOS and a low potential is supplied to a source terminal of the NMOS, the gate terminals of the PMOS and NMOS are connected to each other to form a first input terminal V_{in}, the substrate terminals of the PMOS and NMOS are connected to each other to form a second input terminal when the clock voltages are 0 volt (CLK1=CLK2=0 volt), and the drain terminals of the PMOS and NMOS are connected to each other to form an output terminal V_{out} in figs. 1-4.

Since both Chang et al. and Iwamatsu teach a CMOS device, it would have been obvious to have the circuit connection of Iwamatsu in Chang et al. because the semiconductor structure of Chang et al. can support any desired CMOS wirings connection.

In regards to claim 8, Chang et al. and Iwamatsu differ from the claimed invention by not showing the claimed threshold voltage of each of the P-type semiconductor element and N-type semiconductor element.

It would have been obvious to have the threshold voltage of claim 8 because it depends on the impurity concentrations of the wells and the voltage applied to the second input terminal.

In regards to claim 14, Chang et al. and Iwamatsu differ from the claimed invention by not showing the claimed threshold voltage of each of the P-type semiconductor element and N-type semiconductor element.

It would have been obvious to have the threshold voltage of claim 14 because it depends on the impurity concentrations of the wells and the voltage applied to the second input terminal.

6. Applicant's arguments filed 7/10/02 have been fully considered but they are not persuasive.

It is urged, in pages 7 and 8 of the remarks, that Chang et al. does not disclose or suggest applying an input signal to the regions 28 and 30 and there is no motivation to combine Chang et al. and Iwamatsu. However, the combined device shows all the claimed limitation of the claims and applying an input signal to the regions 28 and 30. As mention in the rejection, it would have been obvious to combine the devices of Chang et al. and Iwamatsu because the well contacts of Chang et al. reduce the electrical resistance between the well terminals and the well. In addition, the electrical insulation layer [14] of Chang et al. insulates all the terminals of the PMOS, NMOS and the wells.

7. Claims 22, 24 and 28 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

8. Claims 10 and 18 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven Loke whose telephone number is (703) 308-4920. The examiner can normally be reached on 7:50 am to 5:20 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

sl
October 5, 2002

Steven Loke
Primary Examiner
Steven Loke